HAPS

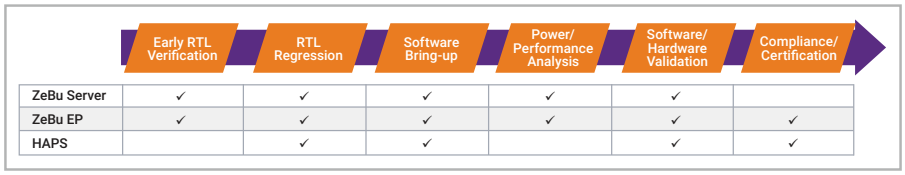
Pre-silicon Prototyping

Synopsys HAPS® prototyping solution dramatically accelerates software development, hardware verification, and system validation from individual IP blocks to processor subsystems to complete SoCs. HAPS is the de facto ASIC Pre-silicon Prototyping platform industry standard across the entire electronic supply chain from IP to semiconductor and system companies.

HAPS prototyping solution consists of proven, robust hardware platforms and HAPS ProtoCompiler prototyping software, which are optimized to deliver the best performance. Solutions are available to support desktop or enterprise configurations. HAPS ProtoCompiler prototyping software builds on 20+ years of FPGA synthesis expertise built with the Synopsys Synplify® FPGA synthesis product line.

Prototyping Use Cases

Synopsys offers the highest-performance Hardware-assisted Verification portfolio, with the most cost-effective platforms to cover all use cases.



ZeBu Server	✓	✓	✓	✓	✓	
ZeBu EP	✓	✓	✓	✓	✓	✓
HAPS		✓	✓		✓	✓

RTL Regression—HAPS is ideal for IP RTL regressions for single-clock IPs. It allows fast execution of hardware and software. It is suitable for CPUs, GPUs, NPUs, and AI-accelerators.

Software Bring-up—HAPS can help validate low-level software drivers before software/hardware validation. Several debug capabilities allow developers to monitor and debug the execution software during the SoC system bring-up.

Software/Hardware Validation—HAPS prototyping systems are used when synthesizable RTL source code of the ASIC/system-on-chip design is available, allowing designers to develop software, verify SoC hardware, and enable system validation before the silicon is taped out.

Compliance/Certification—HAPS prototyping systems are capable of at-speed interface prototyping, due to the asynchronous capabilities of the HAPS ProtoCompiler. The HAPS IP Prototyping Kit offers at-speed prototyping of Synopsys IP, allowing customers to run interoperability testing as well as compliance and certification.

HAPS Product Family

HAPS-100

HAPS-100 is the industry's highest performance and most scalable pre-silicon prototyping system. Synopsys HAPS® is the only platform in the verification flow that ensures all the pieces you design, including at-speed interfaces, work together in the system. Development teams need to get their product out the door with real-world speed interfaces, software, and hardware all working together. Software execution demands require the ability to run long cycles of software workloads, running fast enough to have the hardware validated before the next silicon arrives. HAPS-100 is the best platform for software development use cases.

HAPS-100 1 FPGA	HAPS-100 4 FPGA	HAPS-100 12 FPGA
Desktop form factor in a portable platform. Best debug and performance in the desktop category for the industry	Offers full flexibility for a range of applications, from small designs with multiple users sharing the system to larger designs built up by cabling together multiple systems. Our most popular model is the software workhouse in the industry	High-capacity enterprise solution. Optimized for 1 BG+ designs and suitable for data-center installations
		
Desktop form factor	Desktop or enterprise form factor	Enterprise form factor

Benefits:

- Fastest performance
  - 20-50 MHz for complex SoCs and up to 500 MHz for interface IP
- Asynchronous clocks
- At-speed prototyping interfaces
- Desktop or enterprise form factors

Features:

- Leverage leading-edge interface IP implementation
  - Support for a broad range of interfaces
- Highest performance with support for asynchronous clocking
- The only platform to verify interfaces at-speed.
- The only platform that supports Synopsys PHY IP
- Support fastest software bring-up and software/hardware validation for full RTL models
- Scalable architecture supports multi-BG designs
- 20 years of developing performance-optimized FPGA synthesis software for leading customers

HAPS ProtoCompiler Software

HAPS ProtoCompiler software helps the prototyping team create the fastest performing implementation of their design on the HAPS prototyping hardware. It enables the prototype to find both the optimum partitioning between the FPGAs and the best connectivity using the HapsTrak3 cable. After this is done the ProtoCompiler will use its proven timing-driven synthesis engine to create the optimum prototype. It will handle complicated clocking structures and map them into a performance to optimized prototype.

IP Prototyping Kit

The Synopsys IP Prototyping Kit for HAPS is the only product that can accelerate your schedule by providing immediate, out-of-the-box access to Synopsys Interface IP optimized for FPGA Prototyping. Without this product, customers can spend many months trying to optimize ASIC IP for FPGA prototyping without really knowing the details of how the IP is implemented.

The Synopsys IP Prototyping Kit for HAPS is a pre-optimized kit that can be deployed push-button and can save months of tedious effort. By providing an interface IP Prototype design, SW development teams do not need FPGA expertise to bring up their interface IP prototype. Product schedules can be accelerated when SW development begins prior to full SoC HAPS prototype availability. HW and SW development teams can now work in parallel.